What is claimed is:

1. A communications channel system for using fibre-channel cyclic-redundancy code (CRC) for data integrity in an on-chip memory comprising:

a first channel node having a first port and a second port, each port supporting a fibre-channel arbitrated-loop communications channel, each communications channel including a cyclic-redundancy code within data transmissions on the communications channel;

an on-chip frame memory located on-chip in the first channel node that receives a frame and the received frame's associated CRC from the communications channel; and

an integrity apparatus that uses the received associated CRC for data-integrity checking of the received frame that is in the on-chip frame memory.

3 2. The system according to claim 1, further comprising:

an off-chip memory operatively coupled to the on-chip frame memory and the integrity apparatus; and

a verification circuit within the integrity apparatus that verifies the cyclic-redundancy code while moving the received frame from the on-chip memory to the off-chip memory.

4 3. The system according to claim 3 2, wherein the integrity apparatus checks and strips away the cyclic-redundancy code while moving the received frame to the off-chip memory, the system further comprising

a parity-generation circuit that generates and appends parity to the data as the data are moved from the off-chip memory to the on-chip memory.

5 4. The system according to claim 3 2, wherein a data frame devoid of a cyclic-redundancy code is held in the off-chip memory, the system further comprising:

a CRC generator that generates cyclic-redundancy code based on the data frame from the off-chip memory as the data frame is moved into the data-frame

buffer, and that places the CRC into the on-chip frame memory with the data frame; and

a transmitter that transmits the data frame, including the generated cyclic-redundancy code, onto the communications channel.

7 5. The system according to claim 3 2, wherein a data frame that is to be transmitted is transferred to the on-chip frame memory from the off-chip memory and is stored in the on-chip frame memory with parity but without CRC information.

8 6. The system according to claim 7 5, wherein a received data frame transferred to the on-chip frame memory from the communications channel is stored in the on-chip frame memory with CRC but without parity information.

6 7. The system according to claim 3 2, wherein a received frame transferred to the on-chip frame memory from the communications channel is stored in the on-chip frame memory with CRC but without parity information.

2 8. The system according to claim 1, further comprising:

a magnetic-disc-storage drive operatively coupled to the first channel node; and

a computer system having a second channel node, wherein the second channel node is operatively coupled to the first channel node in a fibre-channel loop in order to transfer data between the first and second channel nodes through the fibre-channel arbitrated-loop communications channel.

9. A disc drive comprising:

a rotatable disc;

a transducer in transducing relationship to the rotating disc;

a channel node having a first port and a second port, each port supporting a fibre-channel arbitrated-loop communications channel, each communications channel including a cyclic-redundancy code within data transmissions on the

communications channel, the channel node operatively coupled to the transducer to communicate data;

an on-chip frame memory located on-chip in the channel node that receives a frame and the received frame's associated CRC from the communications channel; and

an integrity apparatus that uses the received associated CRC for data-integrity checking of the received frame that is in the on-chip frame memory.

10. The disc drive according to claim 9, further comprising:

an off-chip memory operatively coupled to the on-chip frame memory and the integrity apparatus; and

a verification circuit within the integrity apparatus that verifies the cyclic-redundancy code while moving the received frame from the on-chip memory to the off-chip memory.

11. A communications method comprising steps of:

(a) supporting a fibre-channel arbitrated-loop communications channel on each of a first port and a second port of a first channel node;

(b) receiving a frame from the communications channel, the received frame including a cyclic-redundancy code that is based on other data in the received frame;

(c) storing the received frame, including the cyclic-redundancy code, into a frame buffer;

(d) moving the received frame to a memory that is separate from the frame buffer; and

(e) checking the received frame for accuracy by verifying the cyclic-redundancy code (CRC) while moving the received frame to the separate memory.

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~~12.~~ The method according to claim 11, further comprising steps of:

(f) placing a frame that is to be transmitted into an on-chip frame buffer;

(g) generating the cyclic-redundancy code based on data in the frame to be transmitted; and

(h) transmitting the frame to be transmitted, including the cyclic-redundancy code, onto the communications channel.

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~~13~~. The method according to claim ~~12~~, wherein the placing step (f) further includes steps of:

(f)(i) generating parity for data of the frame to be transmitted;

(f)(ii) adding parity to the data of the frame to be transmitted; and

wherein the moving step (d) further includes a step of

(d)(i) stripping away the cyclic-redundancy code while moving the received frame to the separate memory.

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~~14~~. The method according to claim 11, wherein the receiving step (b) further includes a step of

(b)(i) checking the received frame for accuracy by verifying the cyclic-redundancy code while receiving the received frame from the communications channel.

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~~15~~. The method according to claim 11, further comprising a step of

(i) transferring data through the fibre-channel arbitrated-loop communications channel between a magnetic-disc-storage drive that is operatively coupled to the first channel node and a computer system having a second channel node, wherein the second channel node is operatively coupled to the first channel node by the communications channel.

16. A communications channel system comprising:

a channel node having a first port and a second port, each port supporting a fibre-channel arbitrated-loop communications channel, each communications channel including a cyclic-redundancy code within data transmissions on the communications channel;

a buffer that receives, from the channel node, a frame that includes a cyclic-redundancy code;

an off-chip memory separate from the buffer;

means for moving the received frame from the buffer to the off-chip memory and checking the received frame for accuracy by verifying the cyclic-redundancy code (CRC) while moving the received frame to the off-chip memory.

17. The system according to claim 16, wherein the means for moving further includes means for stripping away the CRC as the frame is checked and moved to the off-chip memory.